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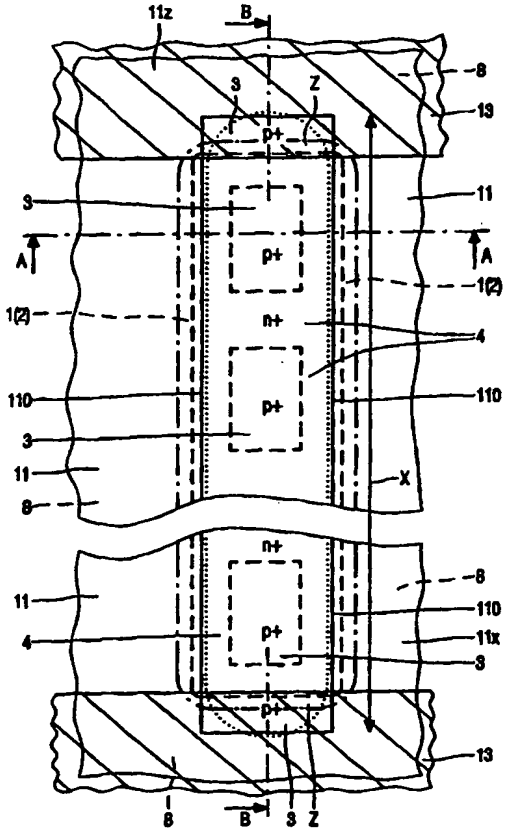
(57) Abstract

A power semiconductor device comprises a multiple–cellular insulated–gate field–effect transistor structure with each cell (100) present at a corresponding opening (110) in a mesh–shaped gate electrode (11). The cells (100) and the openings (110) are of elongate shape having longitudinal sides (X) at which the channel areas (1) are present under a gate insulating layer (12) under longitudinal parts (11x) of the gate electrode (11). The channel areas (1) are absent at ends (Z) of the elongate cells (100). Preferably, the longitudinal parts (11x) of the gate electrode (11) are interconnected beyond the ends (Z) of the elongate cells (100) by interconnection parts (11z) of the gate electrode (11) which are located on a thicker insulating layer (13) than the gate insulating layer (12). This thicker insulating layer (13) is present at least between facing ends (Z) of neigbouring elongate cells (100) where the channel areas (11) are absent.



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DESCRIPTION

POWER SEMICONDUCTOR DEVICES

This invention relates to power semiconductor devices comprising a multiple-cellular insulated-gate field-effect transistor structure, for example MOSFETs (insulated-gate unipolar transistors) or IGBTs (insulated-gate bipolar transistors), or MOS-gated thyristors. The invention also relates to methods of manufacturing such power devices.

Power semiconductor devices are known comprising a multiple-cellular insulated-gate field-effect transistor structure with each cell present at a corresponding opening in a mesh-shaped gate electrode, wherein the gate electrode extends on a gate insulating layer over channel areas of a transistor-body region of one conductivity type in each cell for gating a conduction channel of the opposite conductivity type in the channel area in operation of the device. Published European Patent Application EP-A-0 717 449 discloses such a power semiconductor device in which the cells and the openings in the gate electrode are of elongate shape having longitudinal sides at which the channel areas are present under the gate insulating layer under longitudinal parts of the gate electrode.

In the cellular structure disclosed in EP-A-0 717 449 the channel regions of neighbouring cells are joined along their facing ends so as to eliminate corners at which avalanche current tends to concentrate. Careful control is required for the doping of these channel regions where they join one another. In the EP-A-0 717 449 embodiments, these channel regions are joined by lateral diffusion under interconnection parts of the gate electrode.

It is an aim of the present invention to provide a modified elongate cellular arrangement which mitigates corner effects in a different manner and which can be manufactured in a process-tolerant and versatile manner.

According to a first aspect of the present invention there is provided a

power semiconductor device comprising a multiple-cellular insulated-gate field-effect transistor structure with each cell present at a corresponding opening in a mesh-shaped gate electrode, wherein the gate electrode extends on a gate insulating layer over channel areas of a transistor-body region of one conductivity type in each cell for gating a conduction channel of the opposite conductivity type in the channel area in operation of the device, and wherein the cells and the openings in the gate electrode are of elongate shape having longitudinal sides at which the channel areas are present under the gate insulating layer under longitudinal parts of the gate electrode, characterised in that the channel areas are absent at ends of the elongate cells.

The design and manufacture of such a device in accordance with the present invention adopts an opposite approach to that of EP-A-0 717 449, in that no channel areas are provided at the ends of the elongate cells (instead of joining together channel areas as in EP-A-0 717 449).

The absence of the channel areas from the ends of the elongate cells can be achieved using one or more of a variety of doping, insulation and/or layout techniques. Thus, for example, the techniques used may be an appropriate gate-electrode layout pattern, and/or an appropriate source-region layout pattern, and/or inclusion of a thicker insulating layer than the gate insulating layer, and/or inclusion of a more highly doped region in the transistor-body region.

Thus, in one form, the gate electrode may be absent from the ends of the elongate cells. However, it is advantageous for the longitudinal parts of the gate electrode to be interconnected beyond the ends of the elongate cells by interconnection parts of the gate electrode which can serve to reduce the electrical resistance of the whole gate electrode of the device. These interconnection parts can be located on a thicker insulating layer than the gate insulating layer, the thicker insulating layer being present between facing ends of the neighbouring elongate cells where the channel areas are absent.

This thicker insulating layer may be present only at the ends of the elongate cells where the channel areas are absent. However, it may also extend as thick insulator stripes which are located in-between the longitudinal

sides of neighbouring elongate cells. These thick insulator stripes may be present under a central elongate area of the longitudinal parts of the gate electrode where the gate electrode overlies a semiconductor region of opposite conductivity type between the transistor-body regions of neighbouring cells. Thus, for example, the thick insulating layer itself may be mesh-shaped and may serve to reduce capacitance between the gate electrode and the semiconductor region of opposite conductivity type between the neighbouring cells.

A more highly-doped region of the same conductivity type as the transistor-body regions may be present at each end of the elongate cells and may over-dope the transistor-body regions at these ends to terminate the ends of the elongate cells without channel areas at these ends. This highly doped region may be formed simply as an extension of a highly-doped region provided already in the cells using existing manufacturing processes.

According to a second aspect of the present invention there is provided a method of manufacturing a power semiconductor device in accordance with the first aspect, further characterised by the steps of:

(a) forming, at a surface of a semiconductor body portion, an insulating layer structure comprising a gate insulating layer over where the channel areas are to be provided and comprising a thicker insulating layer where the ends of the elongate cells are to be provided,

(b) depositing a layer of gate-electrode material on the insulating layer structure,

(c) using a photolithographic masking and etching treatment to define a mesh pattern by forming an etchant mask on the layer of gate-electrode material and by etching away unmasked areas of the layer of gate-electrode material and so to form the mesh-shaped gate electrode which has the openings of elongate shape, the longitudinal sides of these openings being present where the channel areas are to be provided, the longitudinal parts of the gate electrode being present on the gate insulating layer and being interconnected by interconnection parts of the gate electrode which are present on the thicker insulating layer,

(d) carrying out a doping step into the semiconductor body portion

where the cells are to be formed so as to provide each cell with the transistor-body regions, wherein the lateral extent of the transistor-body regions is defined by the mesh pattern of step (c) along the longitudinal sides of the elongate cells and is defined by an edge portion of the thicker insulating layer at each end of the elongate cells, which edge portion of the thicker insulating layer is present within the openings in the mesh-shaped gate electrode so as to avoid the formation of the transistor-body regions under the interconnection parts of the gate electrode at the ends of these openings.

Such a method permits the present invention to be realised as a simple modification of existing manufacturing processes.

The step (d) may include carrying out two doping steps into the semiconductor body portion where the cells are to be formed, the two doping steps being with dopant of the same conductivity type but with a higher doping concentration for one of the two doping steps so as to provide each cell also with a more highly-doped region of the same conductivity type as the transistor-body regions. The provision of a more highly doped region of the same conductivity type as the transistor-body regions is already part of existing manufacturing processes. However, in accordance with the present invention, the lateral extent of this more highly doped region may be defined by a mesh pattern of step (c) along the longitudinal sides of the cells and by the edge portion of the thicker insulating layer at each end of the elongate cells.

Depending on the particular etching treatment used to form the mesh-shaped gate electrode in step (c), the elongate openings formed in this electrode may be wider than the openings in the etchant mask. The doping step (d) may comprise a first doping step for providing the more highly doped region and second doping step for providing the transistor-body regions. The lateral extent of the more highly doped region may be defined both by masking with the mesh pattern of the etchant mask and with the edge portion of the thicker insulating layer as in step (d) and by subsequent lateral diffusion in the body portion. This lateral diffusion of the more highly doped region may be sufficient to extend the more highly doped region to beneath the edge portion of the thicker insulating layer, while over-doping the transistor-body regions at the

ends of the elongate cells so terminating the ends of the elongate cells without channel areas.

These and other features in accordance with the present invention, and their advantages, are illustrated specifically in embodiments of the invention now to be described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a plan view of part of the layout of a multiple-cellular insulated-gate field-effect transistor structure in a power semiconductor device in accordance with the present invention;

Figure 2 is an enlarged plan view of the opposite end portions of one of the elongate cells (showing also its semiconductor body regions) of the transistor structure of Figure 1;

Figure 3A is a cross-sectional view on the line A-A of Figure 2;

Figure 3B is a cross-sectional view of the opposite ends of the elongate cell on the line B-B of Figure 2;

Figure 4 is a plan view of a modification of the layout of the transistor structure of Figure 1, illustrating a second embodiment in accordance with the present invention;

Figures 5A and 5B are respective modifications of the cross-sectional views of Figures 3A and 3B, illustrating further modifications in the second embodiment in accordance with the present invention;

Figures 6 to 8 are cross-sectional views of the semiconductor device parts of Figures 3A and 3B, at stages during their manufacture by a method in accordance with the present invention; and

Figures 9A and 9B are modifications of the device structure of Figures 5A and 5B, at a stage of manufacture by a modified method also in accordance with the present invention.

It should be noted that the Figures are diagrammatic and not drawn to scale. Relative dimensions and proportions of parts of these Figures have been shown exaggerated or reduced in size, for the sake of clarity and convenience in the drawings. The same reference signs are generally used to refer to

corresponding or similar features in the different embodiments.

The power semiconductor device of Figures 1 to 3 comprises a multiple-cellular insulated-gate field-effect transistor structure with each cell 100 present at a corresponding opening 110 in a mesh-shaped gate electrode 11. The gate electrode 11 extends on a gate insulating layer 12 over surface areas (which provide channel areas 1) of a transistor-body region 2 of one conductivity type (p-type in the example of Figures 3A and 3B) in each cell 100. The gate electrode 11 serves for gating a conduction channel of the opposite conductivity type (n-type in the specific example) in the channel area 1 in operation of the device. In the specific example illustrated in Figures 1 to 3, the device is of the n-channel enhancement type, in which an n-type conduction channel is induced in the p-type transistor body 2 by the overlying insulated gate electrode 11. The conduction channel is of charge carriers of said opposite conductivity type (i.e electrons in the specific example) from a source region 4 of the transistor structure. The transistor-body regions 2 are provided in a drain drift region 8 of opposite conductivity type (n-type in the specific example) which extends between the transistor-body regions 2 of neighbouring cells 100 to the upper surface of the semiconductor body 10.

The cells 100 and the openings 110 in the gate electrode 11 are of elongate shape having longitudinal sides X at which the channel areas 1 are present under the gate insulating layer 12 under longitudinal parts 11x of the gate electrode 11. In accordance with the present invention, the channel areas 1 are absent at the ends Z of the elongate cells 100. Thus, although the longitudinal parts 11x of the gate electrode 11 are interconnected beyond the ends Z of the elongate cells 100 by interconnection parts 11z of the gate electrode 11, these interconnection parts 11z are located on a thicker insulating layer 13 than the gate insulating layer 12. The thicker insulating layer 13 is present between facing ends Z of neighbouring elongate cells 100 where the channel areas 1 are absent. Furthermore, a more highly doped region 3 (see Figure 3B) of the same conductivity type as the transistor-body regions 2 is present at each end Z of the elongate cells 100 and over-dopes the transistor-

body regions 2 at these ends so as to terminate the ends Z of the elongate cells 100 without channel areas 1 at these ends Z. The conduction channel is unable to be formed at the ends Z of the elongate cells 100 because of (a) the higher doping of the region 3, and (b) the increased thickness of the insulating layer 13, and (c) the cut-back of the interconnection part 11z of the gate electrode 11 from the ends Z. Thus, the interconnection parts 11z overlie the thick insulating layer 13 on the highly doped regions 3 and intermediate drift region 8 (instead of over the gate dielectric 12 on the transistor-body regions 2). With this arrangement and location, the interconnection parts 11c of the gate electrode 11 are unable to induce a conduction channel in the transistor-body region 2 from the source region 4. The source region 4 is therefore inactive (not active) at the ends Z of the elongate cells 100.

The semiconductor body of the device of Figures 1 to 3 typically comprises a highly doped monocrystalline silicon substrate 9 having thereon a lowly doped n-conductivity type silicon epitaxial layer forming the drain drift region 8. The power semiconductor device is of vertical configuration and comprises a very large number (hundreds of thousands) of parallel-connected elongate cells which share a common drain drift region 8. In the case of a MOSFET device, the substrate 9 is of the same conductivity type as the drain drift region 8 and is contacted at its bottom major surface by a drain electrode 31. In the case of an IGBT device, the substrate 9 is of opposite conductivity type and is contacted by an anode electrode 31 at its bottom major surface. Each elongate cell 100 may have the highly doped region 3 extending the length of the cell in addition to being present at both ends Z of the elongate cell 100 to terminate these ends. Thus, the region 3 may extend between the transistor-body regions 2 which are present at the longitudinal sides X of the cell 100. The region 3 extends to the body surface at apertures and/or discontinuities in the source region 4. With this arrangement both the regions 3 and 4 are contacted by an electrode 34 at a window in an insulating layer 22 overlying the gate electrode 11. This electrode 34 is a source electrode of the MOSFET device or a cathode electrode of the IGBT device. The multiple cells 100 of the device are connected in parallel between these electrodes 31 and 34

at the opposite major surfaces of the body 8,9.

In order to distinguish more clearly the various features illustrated in the plan views of Figures 1 and 2 (and 4), the following notations are used: the area of the thick insulator 13 is hatched in one direction; the area of the gate electrode 11 is hatched in the opposite direction in Figure 1 (and Figure 4) but is unhatched in Figure 2; a dotted line (• • •) is used for the outline of the highly doped region 3 in Figure 2; a broken line (– – –) is used for the outline of the source region 4 in Figure 2; and a chain-dot line (– • – • –) is used for the outline of the transistor-body regions 2 in Figure 2. The source region 4 overdopes the region 3 where it overlies the region 3 at the body surface. At the cell ends Z the transistor-body regions 2 are overdoped with the highly doped region 3 as illustrated in Figure 2. The contact window in the insulating layer 22 is not shown in Figure 2. The Figure 3B cross-section on the line B-B of Figure 2 does not extend the full length of Figure 2, but Figure 3B shows only the ends of the cell 100 as far as the first contact of the electrode 34 with both regions 3 and 4.

A specific example of a method of manufacturing the power semiconductor device of Figures 1 to 3 will now be described with reference to Figures 6 to 8, which illustrate the corresponding device structure at successive stages of manufacture. The structures in Figures 6A, 7A and 8A are for the device section of Figure 3A, whereas that in Figures 6B, 7B and 8B are for the device section of Figure 3B. The semiconductor body portion which provides the drain drift region 8 is an n-type silicon epitaxial layer 8' doped with, for example, less than 9×10^{14} phosphorous cm^{-3}. As well known in the art, the doping level depends on the desired blocking voltage of the device and may be about $2 \times 10^{14} cm^{-3}$ for a 600 volt device. The device structure of Figures 6A and 6B is obtained by the steps of:

(a) forming at a surface of the epitaxial layer 8' an insulating layer structure 12,13 of, for example, silicon dioxide which comprises the gate insulating layer 12 over where the cells 100 (and particularly their channel areas 1) are to be provided and the thicker insulating layer 13 where the ends Z of the elongate cells 100 are to be provided,

(b) depositing a layer of gate-electrode material such as polycrystalline silicon on the insulating layer structure 12,13, and

(c) using a photolithographic masking and etching technique to define a mesh pattern 41,11 by forming an etchant mask 41 on the layer of gate-electrode material and by etching away unmasked areas of the gate electrode material to leave the mesh-shaped gate electrode 11.

Typically the thickness of the gate insulating layer 12 is less than 0.3μm (micrometre), for example about 80nm (nanometre), whereas the thickness of the layer 13 is typically in excess of 1μm. The layer providing the gate electrode 11 may typically have a thickness in the range of, for example, 0.5μm to 1μm. The etchant mask 41 shown in Figures 6A and 6B may be typically of photoresist having a thickness of, for example 2μm. An isotropic dry etch may be used to etch the gate-electrode material at the openings 40 in the photoresist mask 41. As a result of undercutting the mask 41, the openings 110 in the gate electrode 11 are wider than the openings 40 in the etchant mask 41. In a specific embodiment, the width of the windows 40 in the photoresist mask 41 may be, for example, 11μm, whereas the width of the openings 110 in the gate electrode 11 may be, for example, 15μm. These openings 40,110 are elongate, and in a specific embodiment the length of the longitudinal sides X may be, for example, typically an order of magnitude greater than the width of these openings. Thus, for example, in a specific embodiment, the openings 110 in the gate electrode 11 may have a width of about 15μm and a length of about 210μm. The longitudinal side of the openings 110 are present where the channel areas 1 of the device are to be provided. The longitudinal parts 11x of the gate electrode 11 between the openings 110 are present on the gate insulating layer 12. The interconnection parts 11z of the gate electrode 11 are present on the thicker insulating layer 13. The openings 40 and 110 expose end portions of the thick insulating layer 13, as illustrated in Figure 6B.

In this embodiment of Figures 6A and 6B, a first doping step is carried out before the removal of the etchant mask 40. As represented by the arrows 53 in Figures 6A and 6B, this doping step comprises the implantation of dopant ions, for example of boron, into the epitaxial layer 8' where the device cells 100

are to be formed. This ion implantation serves to provide each cell 100 with the doping for its region 3. In a specific embodiment the boron ion dose for the regions 3 is, for example, in the range of 5 x $10^{14}cm^{-2}$ to 2 x $10^{15}cm^{-2}$. The photoresist mask 41 and the thick insulating layer 13 each have a thickness sufficient to mask the underlying semiconductor body portion 8' against implantation of the boron ions 53. Thus, the lateral extent of the regions 3 as initially implanted is defined by the mesh pattern of the photoresist mask 41 along the longitudinal sides X of the elongate cells 100 as illustrated in Figure 6A and is defined by an edge portion of the thick insulating layer 13 at each end Z of the elongate cells 100 as illustrated in Figure 6B.

After stripping the photoresist mask 41 in known manner, the implanted dopant 53 in the layer 8' is annealed by heating the body 8,9 to 1100°C. This heating treatment causes some diffusion (including lateral diffusion) of the dopant 53 so that the resulting region 3 extends beneath the edge of the thick insulating layer 13 at the ends Z of the cells 100, as illustrated in Figure 7B. Then, as illustrated by arrows 52 in Figures 7A and 7B, a second doping step is carried out for providing the transistor-body regions 2. This doping step also comprises the implantation of boron ions 52. The boron ion dose in this case may be in the range of, for example, 3 x 10^{13} to 5 x $10^{14}cm^{-2}$. The lateral extent of the implant is defined by the sides of the gate electrode 11 along the longitudinal sides X of the elongate cells 100 as illustrated in Figure 7A and is defined by the edge portion of the thick insulating layer 13 at each end Z of the elongate cells 100 as illustrated in Figure 7B. The same implantation window may be used for dopant ions 54 of the opposite conductivity type for forming source regions 4 with the transistor-body regions 2. The implants 52 and 54 are annealed by heating the body structure to 900°C. This heating treatment causes some diffusion (including lateral diffusion) of the implanted dopant 52 and 54 (and also the dopant 53 of region 3) so that the resulting transistor-body region 2 extends beneath the edge of the gate electrode 11 to form the channel areas 1 along the longitudinal sides X (see Figure 8A), between the resulting source region 4 and the drain drift region 8. Some diffusion also occurs beneath the edge of the thick insulating layer 13 at the ends Z of the cells 100 (see

Figure 8B), but in this area the transistor-body region 2 is overdoped by the higher-doped region 3 which already extends beneath the edge of the thick insulating layer 13 at the ends Z of the cells 100. Thus, the region 2 is not formed at the ends Z. The implanted source region 4 is of a higher doping concentration than the highly doped region 3 and so is not overdoped by the region 3.

Figures 8A and 8B illustrate a subsequent stage in the manufacture in which selected areas of the source region 4 are removed to permit the source electrode 34 to contact both the source region 4 and the highly doped region 3 at the semiconductor body surface. In the form illustrated in Figures 8A and 8B, this removal is effected using an etchant mask 44 of, for example, photoresist. In the embodiment shown by way of example in Figures 8A and 8B, the photoresist mask 44 is provided on an insulating layer 22 (for example of silicon dioxide) over the device structure. The selected areas of the source region 4 and overlying areas of the insulating layers 12 and 22 can be removed at the windows 45 in the photoresist mask 44 using an anisotropic etching treatment (for example plasma etching). Subsequently, the insulating layers 12 and 22 may be cut back at the windows 45 using a wet isotropic etch so as to expose surface areas of the source regions 4. After removal of the photoresist mask 44, metallisation such as aluminium can be deposited to form the electrode 34.

Many modifications and variations are possible within the scope of the present invention. Thus, in the embodiments of Figures 1 to 3, the thicker insulating layer 11 is in the form of a stripe which extends only at and between facing ends Z of neighbouring elongate cells 100. Figures 4, 5A and 5B illustrate a modification in which the thick insulating layer 13 is mesh-shaped in comprising further stripes 13x which are located in-between the longitudinal sides X of neighbouring elongate cells 100. These thick insulator stripes 13x are present under a central elongate area of the longitudinal parts 11x of the gate electrode 11 where the gate electrode 11 overlies the drain drift region 8. A lower gate-drain capacitance can be achieved by the inclusion of these stripes 13x.

Figures 5A and 5B also illustrate a further modification in which the

source region 4 of each cell is absent from the ends Z of the cell. Thus, the inactive parts of the source region 4 of the Figure 1 device at the ends Z may be omitted. The resulting source region 4, as in Figures 5A and 5B, may be in the form of two parallel stripe portions 4a and 4b which are parallel to the longitudinal sides X of the elongate cell 100. These stripe portions 4A and 4B terminate short of the ends Z, as illustrated in Figure 5B. The highly doped region 3 extends to the body surface at the ends Z and also in-between the stripe portions 4a and 4b. The stripe portions 4A and 4B may be wholly separated from each other, or they may be joined to each other at intermediate positions along the elongate cell 100 by cross-portions 4c, as illustrated in Figure 4. In this embodiment, as illustrated in Figures 9A and 9B, a masking pattern 46 (of, for example, photoresist) may be used to define the lateral extent of the source region 4, instead of using the etchant mask 44.

Thus, the doping concentration for the source region 4 may be provided by implantation of dopant ions 54 at an implantation window which is defined by the gate electrode 11 along the longitudinal sides X of the cells 100 and by the additional mask 46 at the ends Z of the cells 100 and at intermediate positions along the cells 100. Thus, in the embodiment illustrated in Figure 9B, the additional (photoresist) masking pattern 46 extends into the window in the thick insulating layer 13 at the ends Z of the cells 100. However, it is also possible to terminate the (photoresist) masking pattern 46 on the thick insulating layer 13 at the ends Z of the cells 100. In this case the edge of the thick insulating layer 13 at the ends Z may be used to mask the region 3 at the ends Z against implantation of the dopant ions 54 so as to prevent formation of the source region at the ends Z of the cells 100.

The embodiments of Figures 1 to 9 have been described in terms of a MOSFET device or an IGBT device. By modifying the doping concentrations and dimensions of, especially, the regions 2 and 8, the present invention may be used with a MOS-gated thyristor device having its channel regions 1 absent from the ends Z of elongate cells 100. Although n-channel devices have been described, the present invention may (of course) be applied to p-channel devices, in which the conductivity types of the various regions 2, 3, 4, 8 and 9

are reversed.

From reading the present disclosure, other modifications and variations will be apparent to persons skilled in the art. Such modifications and variations may involve equivalent features and other features which are already known in the art and which may be used instead of or in addition to features already disclosed herein. Although claims have been formulated in this Application to particular combinations of features, it should be understood that the scope of the disclosure of the present application includes any and every novel feature or any novel combination of features disclosed herein either explicitly or implicitly and any generalisation thereof, whether or not it relates to the same invention as presently claimed in any Claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The Applicants hereby give notice that new claims may be formulated to such features and/or combinations of such features during prosecution of the present application or of any further application derived therefrom.

CLAIMS

1. A power semiconductor device comprising a multiple-cellular insulated-gate field-effect transistor structure with each cell present at a corresponding opening in a mesh-shaped gate electrode, wherein the gate electrode extends on a gate insulating layer over channel areas of a transistor-body region of one conductivity type in each cell for gating a conduction channel of the opposite conductivity type in the channel area in operation of the device, and wherein the cells and the openings in the gate electrode are of elongate shape having longitudinal sides at which the channel areas are present under the gate insulating layer under longitudinal parts of the gate electrode, characterised in that the channel areas are absent at ends of the elongate cells.

2. A device as claimed in Claim 1, further characterised in that the longitudinal parts of the gate electrode are interconnected beyond the ends of the elongate cells by interconnection parts of the gate electrode which are located on a thicker insulating layer than the gate insulating layer, the thicker insulating layer being present between facing ends of neighbouring elongate cells where the channel areas are absent.

3. A device as claimed in Claim 2, further characterised in that the thicker insulating layer also extends as thick insulator stripes which are located in between the longitudinal sides of neighbouring elongate cells, the thick insulator stripes being present under a central elongate area of the longitudinal parts of the gate electrode where the gate electrode overlies a semiconductor region of opposite conductivity type between the transistor-body regions of neighbouring cells.

4. A device as claimed in any one of Claims 1 to 3, further characterised in that a more highly doped region of the same conductivity type as the transistor-body regions is present at each end of the elongate cells and over-dopes the transistor-body regions at these ends to terminate the ends of

the elongate cells without channel areas at these ends.

5. A device as claimed in Claim 4, further characterised in that the more highly doped region extends the length of its respective elongate cell in between the transistor-body regions at the longitudinal sides of the cell and is present at both ends of the elongate cell to terminate these ends.

6. A device as claimed in any one of Claims 1 to 5, further characterised in that each cell includes a source region of said opposite conductivity type comprising stripe portions which are parallel to the longitudinal sides of the elongate cell and absent from the ends of the elongate cell.

7. A method of manufacturing a power semiconductor device as claimed in Claim 1, further characterised by the steps of:

(a) forming, at a surface of a semiconductor body portion, an insulating layer structure comprising a gate insulating layer over where the channel areas are to be provided and comprising a thicker insulating layer where the ends of the elongate cells are to be provided,

(b) depositing a layer of gate-electrode material on the insulating layer structure,

(c) using a photolithographic masking and etching treatment to define a mesh pattern by forming an etchant mask on the layer of gate-electrode material and by etching away unmasked areas of the layer of gate-electrode material and so to form the mesh-shaped gate electrode which has the openings of elongate shape, the longitudinal sides of these openings being present where the channel areas are to be provided, the longitudinal parts of the gate electrode being present on the gate insulating layer and being interconnected by interconnection parts of the gate electrode which are present on the thicker insulating layer,

(d) carrying out a doping step into the semiconductor body portion where the cells are to be formed so as to provide each cell with the transistor-body regions, wherein the lateral extent of the transistor-body regions is defined by

the mesh pattern of step (c) along the longitudinal sides of the elongate cells and is defined by an edge portion of the thicker insulating layer at each end of the elongate cells, which edge portion of the thicker insulating layer is present within the openings in the mesh-shaped gate electrode so as to avoid the formation of the transistor-body regions under the interconnection parts of the gate electrode at the ends of these openings.

8. A method as claimed in Claim 7, further characterised in that the step (d) includes carrying out two doping steps into the semiconductor body portion where the cells are to be formed, the two doping steps being with dopant of the same conductivity type but with a higher doping concentration for one of the two doping steps so as to provide each cell also with a more highly doped region of the same conductivity type as the transistor-body regions, wherein the lateral extent of the more highly doped region is defined by a mesh pattern of step (c) along the longitudinal sides of the elongate cells and is defined by the edge portion of the thicker insulating layer at each end of the elongate cells.

9. A method as claimed in Claim 8, further characterised in that the mesh-shaped gate electrode is formed in step (c) with elongate openings which are wider than the openings in the etchant mask, and in that the two doping steps of (d) comprise a first doping step for providing the more highly doped region and a second doping step for providing the transistor-body regions, wherein the lateral extent of the more highly doped region is defined both by masking with the mesh pattern of the etchant mask and with the edge portion of the thicker insulating layer as in step (d) and by subsequent lateral diffusion in the body portion, which lateral diffusion of the more highly doped region is sufficient to extend the more highly doped region to beneath the edge portion of the thicker insulating layer while overdoping the transistor-body regions at the ends of the elongate cells so terminating the ends of the elongate cells without channel areas.

10. A method as claimed in any one of Claims 7 to 9, further

characterised in that a doping concentration of said opposite conductivity type is introduced into the semiconductor body portion for forming source regions with the transistor-body regions, and in that the ends of the elongate cells are masked against said doping concentration of said opposite conductivity type so as to form the source region of each cell with stripe portions which are parallel to the longitudinal sides of the elongate cell and absent from the ends of the elongate cell.

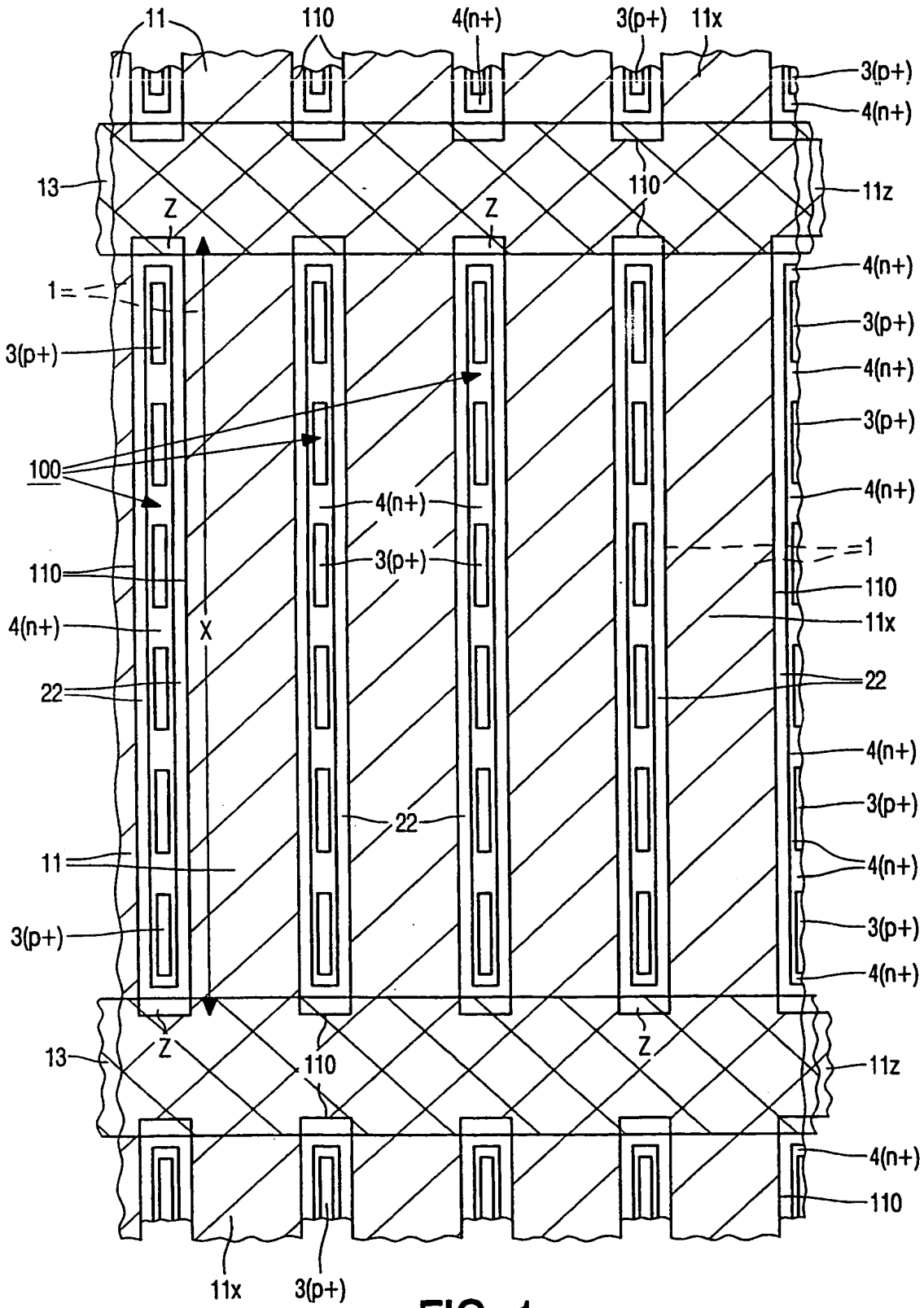

FIG. 1

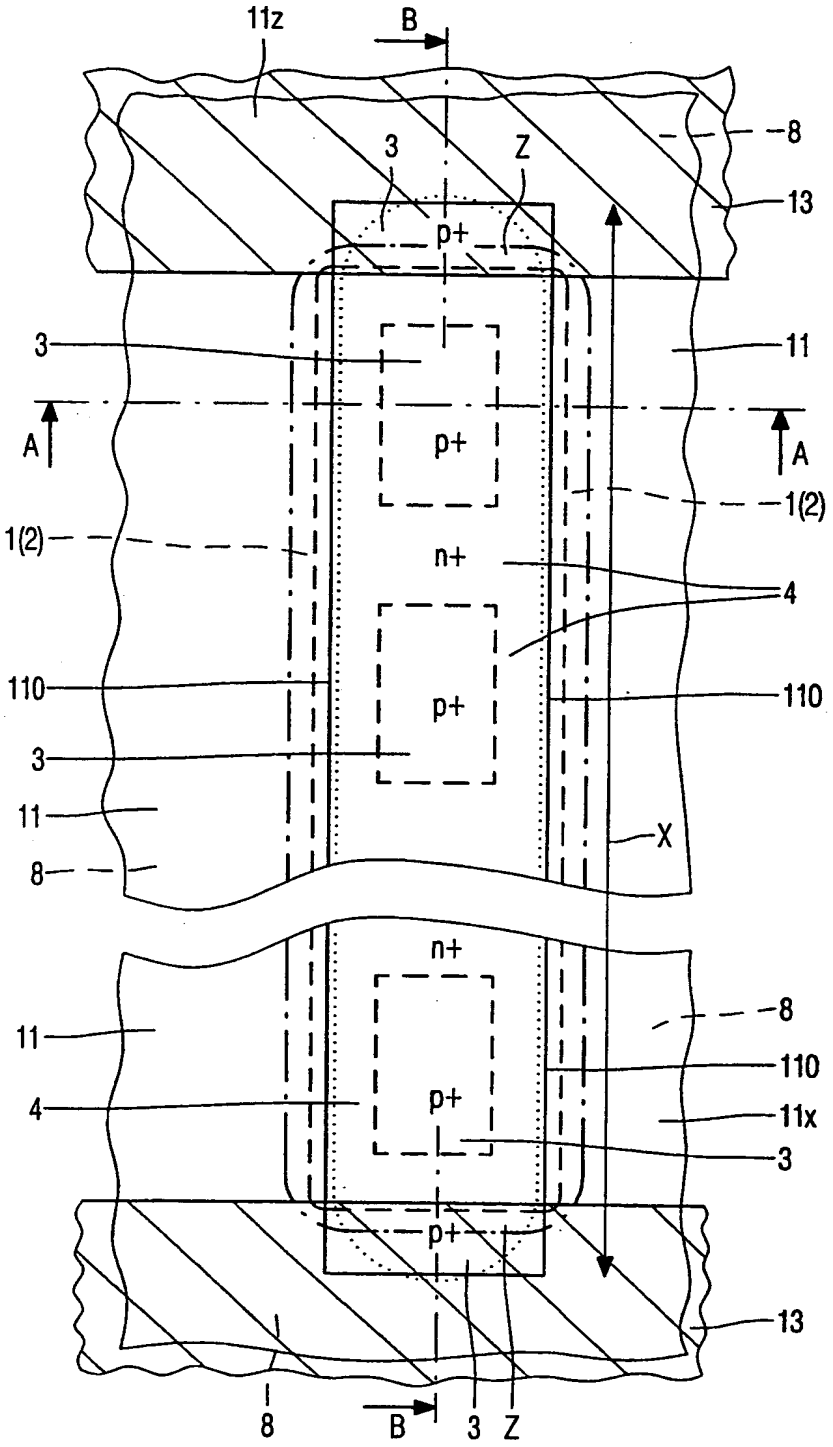

FIG. 2

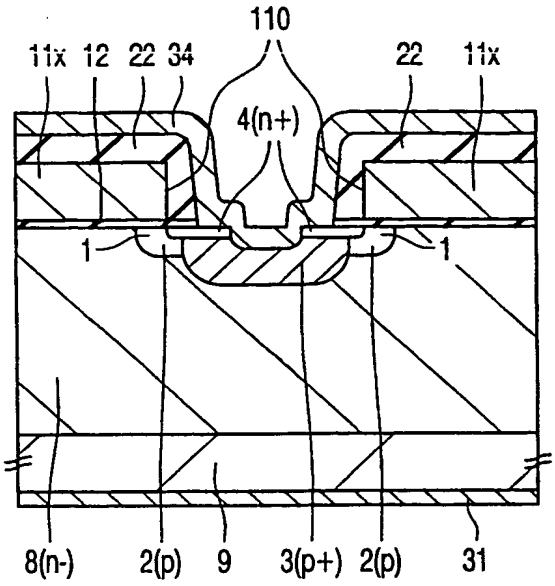

FIG. 3A

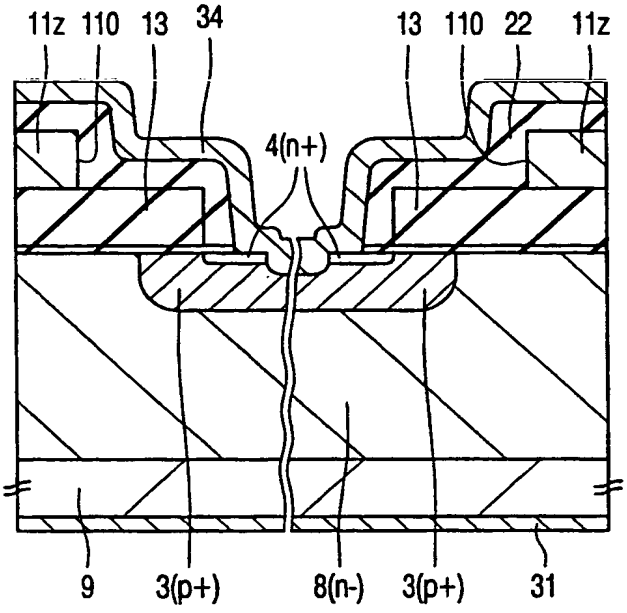

FIG. 3B

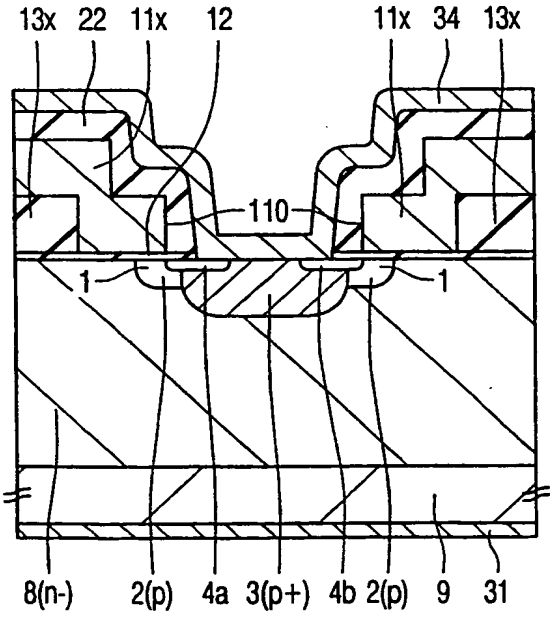

FIG. 5A

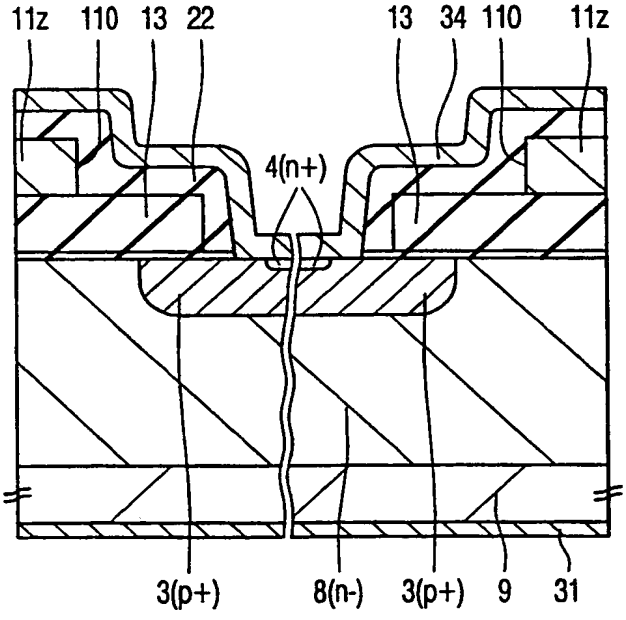

FIG. 5B

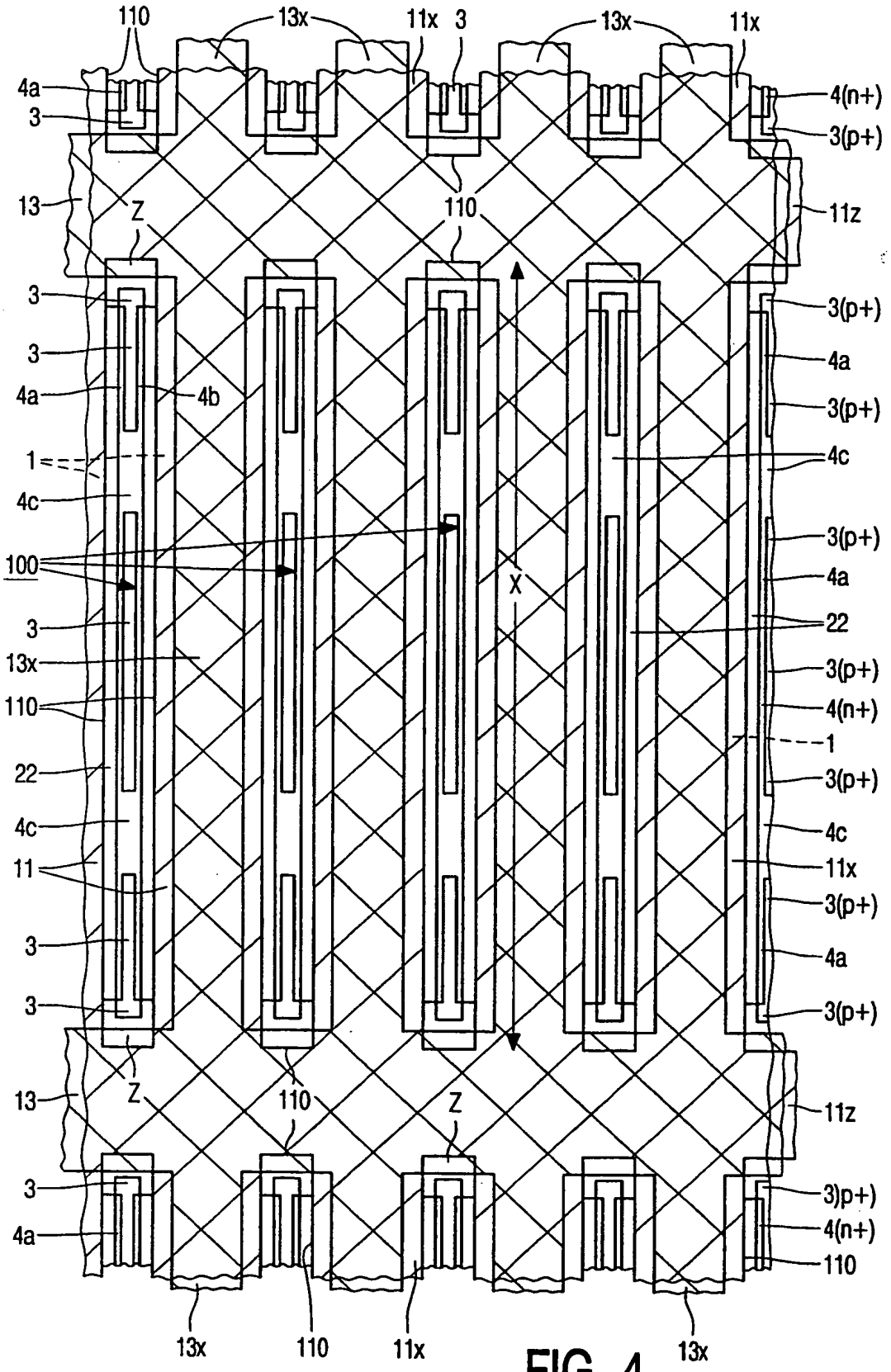

FIG. 4

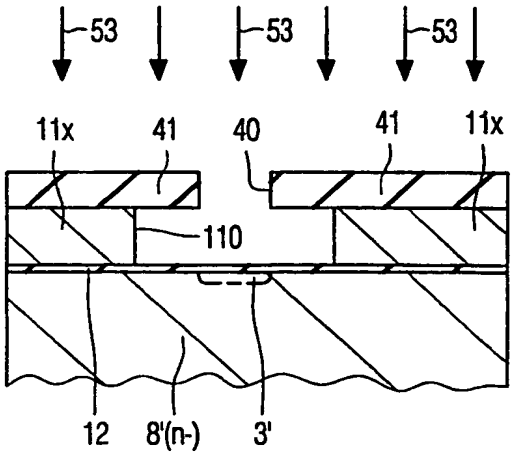

FIG. 6A

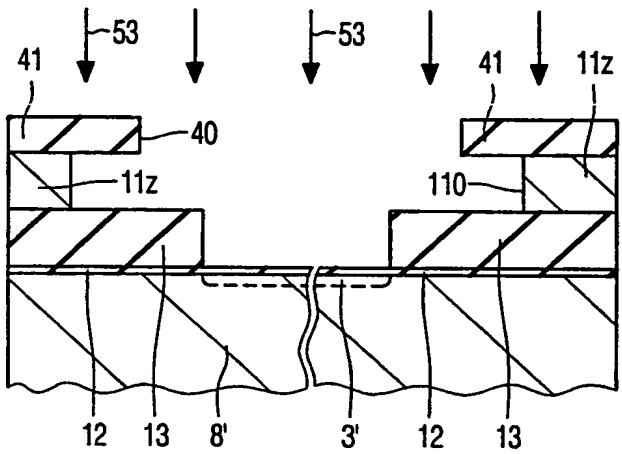

FIG. 6B

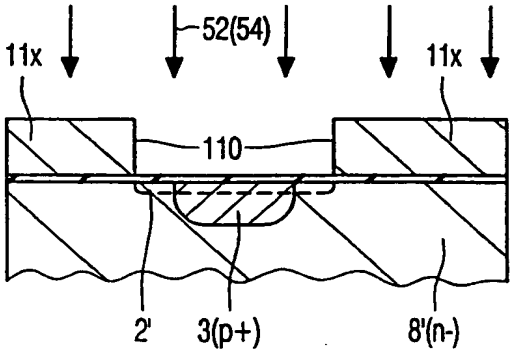

FIG. 7A

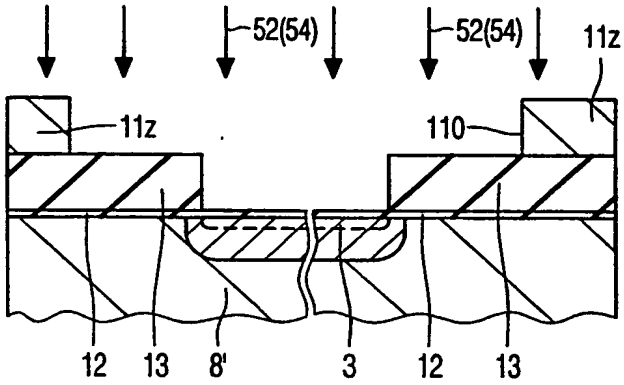

FIG. 7B

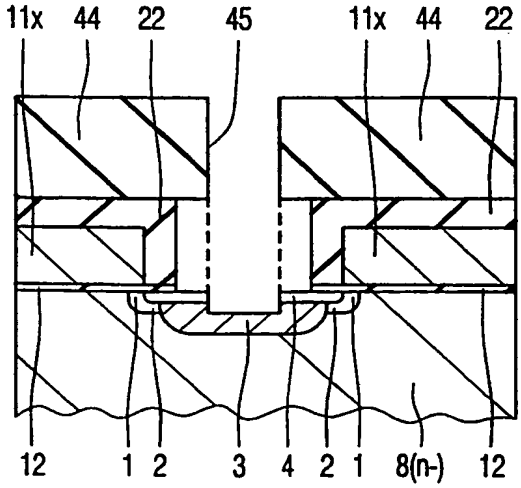

FIG. 8A

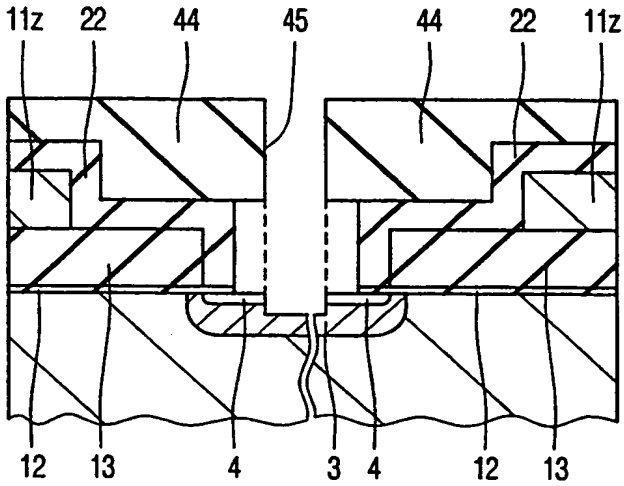

FIG. 8B

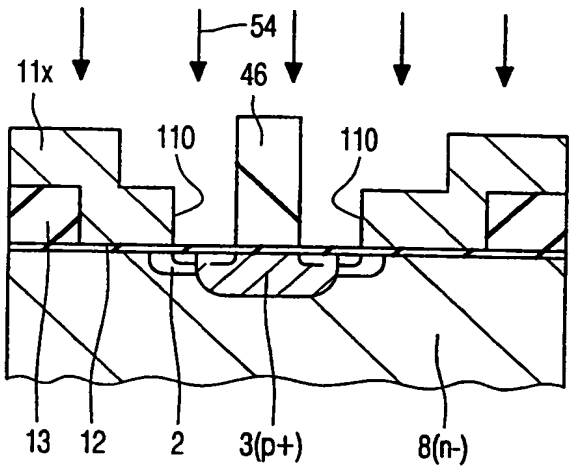

FIG. 9A

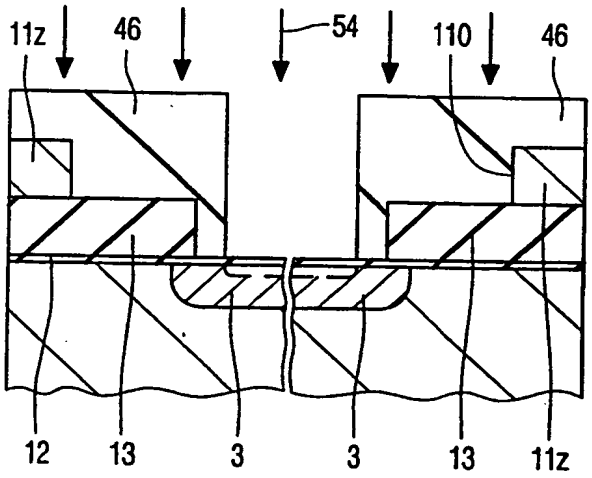

FIG. 9B

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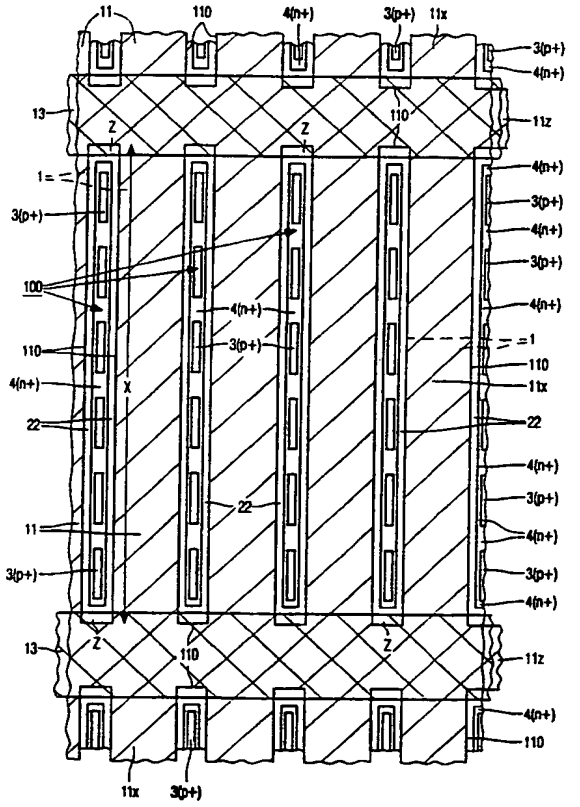
(54) Title: POWER SEMICONDUCTOR DEVICES

(57) Abstract

A power semiconductor device comprises a multiple–cellular insulated–gate field–effect transistor structure with each cell (100) present at a corresponding opening (110) in a mesh–shaped gate electrode (11). The cells (100) and the openings (110) are of elongate shape having longitudinal sides (X) at which the channel areas (1) are present under a gate insulating layer (12) under longitudinal parts (11x) of the gate electrode (11). The channel areas (1) are absent at ends (Z) of the elongate cells (100). Preferably, the longitudinal parts (11x) of the gate electrode (11) are interconnected beyond the ends (Z) of the elongate cells (100) by interconnection parts (11z) of the gate electrode (11) which are located on a thicker insulating layer (13) than the gate insulating layer (12). This thicker insulating layer (13) is present at least between facing ends (Z) of neigbouring elongate cells (100) where the channel areas (11) are absent.



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INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 98/02027

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H01L 29/78, H01L 29/423
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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPAT, WPI, JAPIO

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	EP 0665595 A1 (FUJI ELECTRIC CO. LTD.), 2 August 1995 (02.08.95) --	1-10
A	EP 0717449 A2 (FUJI ELECTRIC CO. LTD.), 19 June 1996 (19.06.96) --	1-10
A	EP 0749163 A2 (FUJI ELECTRIC CO. LTD.), 18 December 1996 (18.12.96) --	1-10

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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Benny Andersson/MN Telephone No. +46 8 782 25 00

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		US 5723890 A	03/03/98
		US 5757046 A	26/05/98